WHAT IS CLAIMED IS:

1. A semiconductor memory device, which includes:

a cell block composed of several series-connected units having a ferroelectric capacitor and a cell transistor parallel-connected to the ferroelectric capacitor; and

a select transistor connected to an end of the cell block,

the semiconductor memory device comprising:

a semiconductor substrate;

a plurality of first impurity diffusion layers formed on the surface of the semiconductor substrate in a state of being mutually separated along a first direction, having a first area, and constituting a source/drain diffusion layer of the cell transistor;

a second impurity diffusion layer formed on the surface of the semiconductor substrate in a state of being separated from the first impurity diffusion layer of an end of the first impurity diffusion layers, having a second area, and constituting a source/drain diffusion layer of the cell transistor;

a plurality of first gate electrodes provided on the semiconductor substrate with a gate insulating film interposed therebetween between the first impurity diffusion layers along a second direction, and constituting a gate of the cell transistor;

a second gate electrode provided on the semiconductor substrate with a gate insulating film

interposed therebetween between the first impurity diffusion layer of the end and the second impurity diffusion layer along a second direction, and constituting a gate of the select transistor; and

a contact electrically connecting a bit line and the second impurity diffusion layer.

2. The device according to claim 1, further comprising:

a plurality of ferroelectric capacitors having both terminals connected to the first impurity diffusion layers on both sides of the first gate electrode, and having a ferroelectric film, and first and second electrodes sandwiching the ferroelectric film.

3. The device according to claim 1, wherein the first impurity diffusion layers have a first length in the first direction, and the second impurity diffusion layer has a second length shorter than the first length in the first direction.

4. The device according to claim 1, wherein the first impurity diffusion layer have a third length in the second direction, the second impurity diffusion layer has a first region electrically connected to the contact, and the first region has a fourth length shorter than the third length in the second direction.

5. The device according to claim 4, wherein the second impurity diffusion layer has a second region

extending along the second direction of the second gate electrode, and the second region has the third length.

6. The device according to claim 4, wherein the first region reaches the second gate electrode.

7. The device according to claim 6, wherein the first impurity diffusion layer of the end has a third region extending along the second direction of the second gate electrode, the third region has a fifth length shorter than the third length.

8. The device according to claim 7, wherein the fifth length is the same as the fourth length.

9. The device according to claim 7, further comprising:

an impurity region formed on the surface of the semiconductor substrate between the first and third regions, and controlling a threshold voltage of the select transistor.

10. The device according to claim 7, further comprising:

a control section applying a first voltage for turning on the cell transistor to the first gate electrode, and applying a second voltage larger than the first voltage for turning on the select transistor to the second gate electrode.